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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: J.A. De Coster et al.

Examiner: Guerrero

Application No.: 09/807,067

Art Unit: 2822

Filed: April 6, 2001

For: METHOD OF MANUFACTURING AN INTEGRATED CIRCUIT COMPRISING
AN IMPROVED SILICIDATION AND A CORRESPONDING INTEGRATED
CIRCUIT

Box AF
Commissioner for Patents
Washington D.C. 20231

FAX RECEIVED

JAN 28 2003

RULE 116 AMENDMENT

TECHNOLOGY CENTER 2800

Sir:

In response to the Final Office Action of December 17, 2002, Applicants respectfully request that the above-identified application be reconsidered in view of the amendments and remarks that follow, and that the application be passed to issue.

In the Claims

Please amend the claims as follows:

1. (TWICE AMENDED) A method of manufacturing an integrated circuit, which method includes a stage wherein lateral isolation regions (spacers) are formed at the sides of a projecting polysilicon region so as to be in contact therewith, said lateral isolation regions each being composed of a smaller isolation layer (402) that is formed by depositing an

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